MSI HIGH SPEED LOW POWER GaAs ICs USING SCHOTTKY DIODE FET LOGIC*

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ABSTRACT

A new approach to the design and fabrication of planar high speed GaAs integrated circuits is described. Experimental digital circuits of MSI level complexities have been fabricated showing high gate density, low dynamic switching energies and very high switching speeds.

Introduction

In 1978, at the ISSCC,[1] a new circuit approach to GaAs digital integrated circuits was presented. This approach referred to as Schottky Diode FET Logic (SDFL), utilizes small area, high conductance, ultra-low capacitance Schottky diodes to perform most logic functions. Inversion and current gain are obtained from depletion-mode (normally-on) GaAs FET's with 1μm gate length. Low power dissipation (0.2 to 2 mW/gate) is obtained by utilizing low pinch-off voltage FETS (0.5 to 1.5 volts). High gate densities (5×10^4 to $10^5/cm^2$) are achieved by use of a planar fabrication process that employs multiple, localized ion implantation, projection photolithography and dry etching techniques. Logic gate propagation delays of 100 ps have been obtained, comparable to those of previously reported depletion-mode GaAs FET IC's,[2] but dissipating almost two orders of magnitude less power. The above conditions will permit the extension of high performance GaAs IC circuit complexities into the LSI range, without sacrificing switching speed or noise margin as is the case for ultra-low power enhancement-mode logic approaches.[3,4]

In this paper, successful fabrication and operation of much more complex sequential and combinatorial logic functions than the initially reported ring oscillators[1] are presented. MSI circuits with more than 60 gates per chip will be discussed.

Circuit Approach

Figure 1 shows a circuit diagram of a 2 input Schottky Diode FET Logic NOR gate. In this gate, the logical OR function is provided by the 1μm x 2μm Schottky diodes D_A and D_B which have junction capacitances of 2 fF and series resistances as low as 300Ω. These diodes require a deep (~0.5μm) low sheet resistance implant for their fabrication, whereas the low power, high transconductance GaAs MESFETs require a very shallow (0.1μm), higher sheet resistance implant. As a consequence, SDFL circuits cannot be fabricated by the mesa-epitaxial or mesa-uniform implant fabrication techniques used for GaAs microwave FETs. Input expansion is easily provided by additional logic diodes. Small gate area is maintained, since the extremely small 2-terminal logic diodes require many fewer overcrossings than FET's or other 3-terminal active logic elements. These diodes also provide some (or all) of the level shifting required between drain and gate in depletion-mode logic. The pulldown active load (PD) provides the bias current for the logic diodes and most of the current required to turn off the gate of Q1. Fanout of the basic NOR gate is limited to 3 or 4 by the ratio of PD and PU currents. However, fanout expansion can easily be achieved, when necessary, by utilizing larger source followers or inverters as output buffers. Also, larger single NOR gates can be constructed for higher fanout requirements by scaling of FET channel widths. NOR gates composed of 5, 8, 10, 15 and 20μm wide FETs have been fabricated and tested.

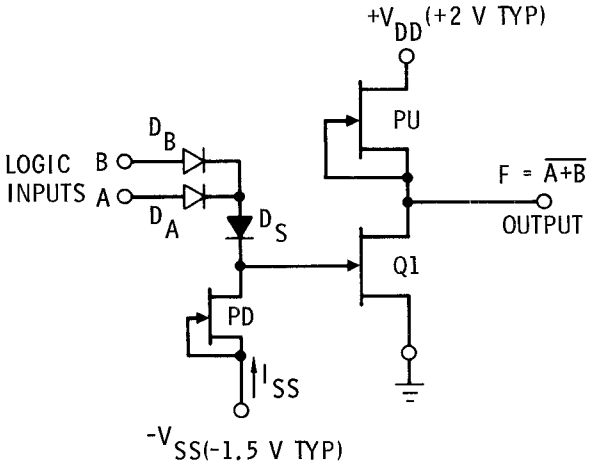

Fig. 1 Schottky Diode FET Logic NOR Gate

Ring oscillators, consisting of chains of odd numbers of logic gates, are used to evaluate propagation delay (τ_d) and dynamic switching energy ($P_D\tau_D$) of the SDFL logic gates. Five micron NOR gates have yielded dynamic switching energies as low as 27 fJ/-gate with 156 ps propagation delay while 20μm NOR gates have provided 75 ps propagation delay and 170 fJ/gate dynamic switching energy.[5] The speed and power are strongly influenced by gate widths, pinchoff voltage and gate area.

MSI Circuit Evaluation

Circuits in the MSI range of complexity have been designed and fabricated using the planar SDFL approach. All high speed measurements required for testi testing the circuits have been made at wafer probe level. Output buffers (source followers) are located on-chip to prevent loading of the circuit during testing. Binary ripple counters or frequency dividers have been made using the D Flip-Flop (DFF) as a basic building block. The DFF contains 6 NOR gates, interconnected to form 3 set-reset latches. By connecting the D (data) input to the Q output, the clock input will produce an output transition for every full clock cycle. Thus, each DFF stage divides by 2. Clock rates up to 1.875 GHz have been achieved on single DFF dividers, corresponding to an equivalent propagation delay of 110 ps, in good agreement with ring oscillator data. The power dissipation for this DFF was 15 mW. Therefore, the dynamic switching energy was 0.28 pJ/gate. Power dissipations as low as 4.5 mW or 0.75 mW/gate have been observed for DFF dividers fabricated on low pinchoff voltage wafers.

Three stage dividers (divide by 8) containing 25 NOR gates have also been fabricated and were evaluated

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up to 1.1 GHz clock frequencies. Total power dissipation was 45 mW, corresponding to 10 mW per DFF. The divided output spectrum showed very good noise properties, with a noise-to-carrier ratio of at least -100 dB at a 1 MHz baseband frequency. This ratio was limited by the dynamic range of the spectrum analyzer, not necessarily by the divider.

In addition, larger MSI circuits including an 8 input data multiplexer containing 64 gates has been evaluated. A schematic diagram of this circuit is shown in Fig. 2, and an SEM photograph of a multiplexer chip is shown in Fig. 3. This circuit utilizes a three stage, DFF implemented, synchronous counter as an address generator for the multiplexer gate array. The data output of the multiplexer is latched using another DFF stage to prevent glitching. Operation of this multiplexer has been achieved at a clock frequency of 1.04 GHz. Figure 4 shows the output of the multiplexer at 225 MHz with inputs 3 and 5 biased at V_{DD} and all others at ground. This results in the repetitive bit pattern shown when the multiplexer is clocked. The sync output of a multiplexer at an 866 MHz clock rate is shown in Fig. 5. Power dissipation of the multiplexer circuits varied from 75 mW to 375 mW for wafers with pinchoff voltages of 0.5V and 1.45V, respectively.

A 1 input to 8 output data demultiplexer containing 60 gates was also fabricated and evaluated. The circuit design used for this device is quite similar to the data multiplexer. A synchronous counter provides the address for selecting 1 out of 8 NOR gates sharing a common data input. Operation of this circuit has been demonstrated at a clock frequency of 1.06 GHz. An output waveform, measured on a sampling oscilloscope, for the sync output of the demultiplexer with the input biased at V_{DD} is shown in Fig. 6. Here, a clock frequency of 880 MHz was used. Bandwidth of the measurement system was limited to 900 MHz by the Tektronix FET probe used to buffer the output of the demultiplexer.

Conclusion

These initial results on depletion-mode GaAs MESFET IC's at the MSI level of complexity indicate that the high density, planar, SDFL circuit approach shows excellent promise for extension into high performance LSI logic circuits.

Acknowledgements

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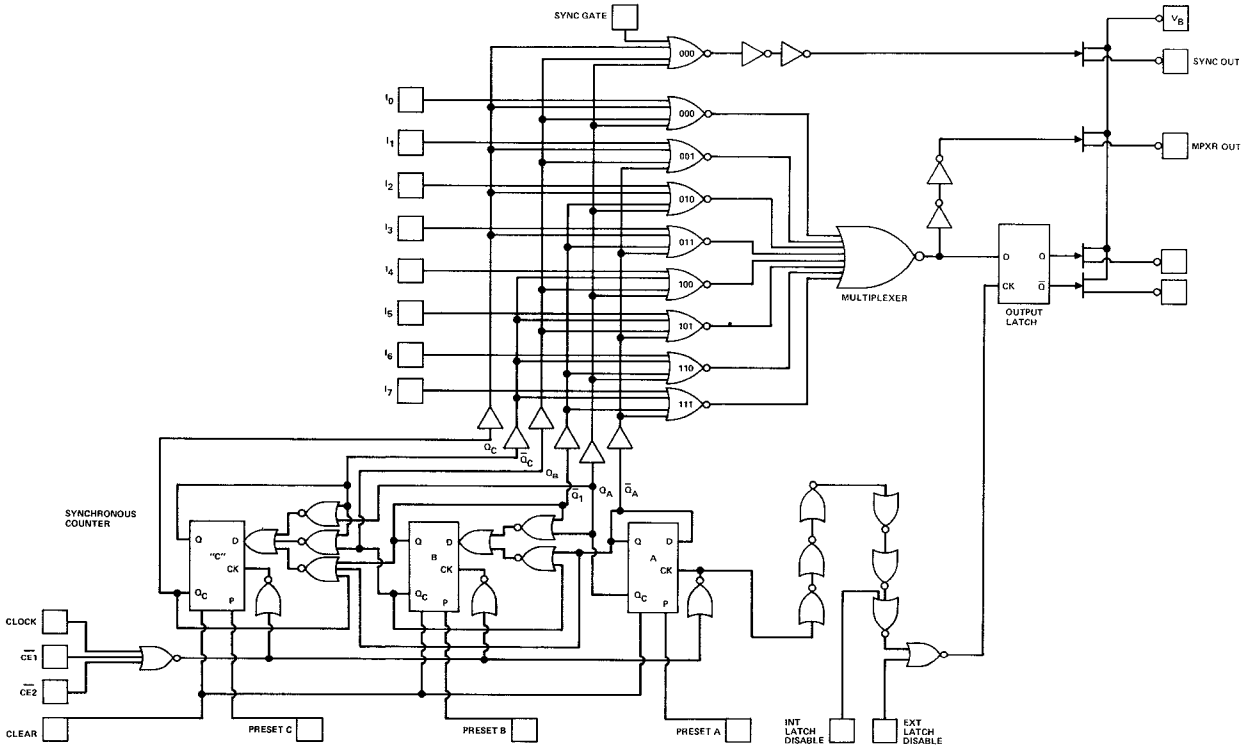

Fig. 2 Eight Input Data Multiplexer

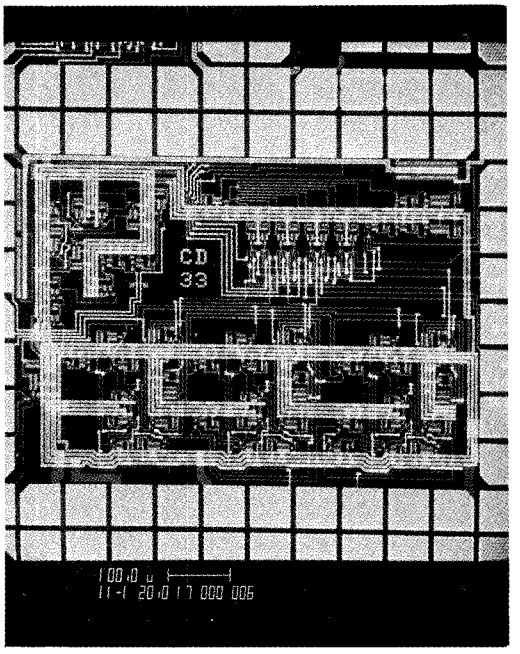

Fig. 3 SEM Photograph of 8 Input Data Multiplexer

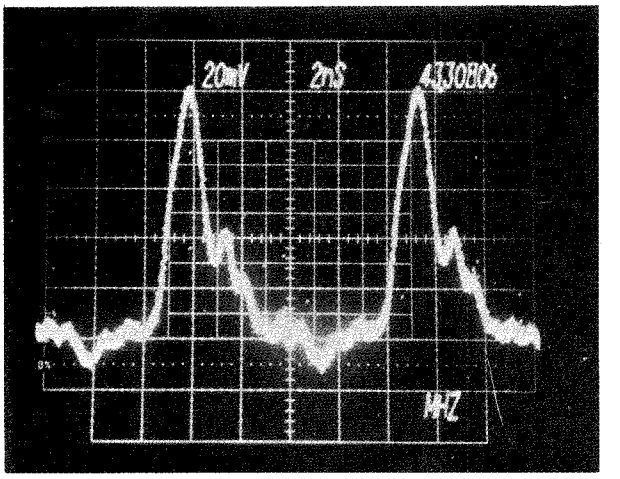

Fig. 5 Multiplexer Sync Output at 866 MHz Clock Frequency

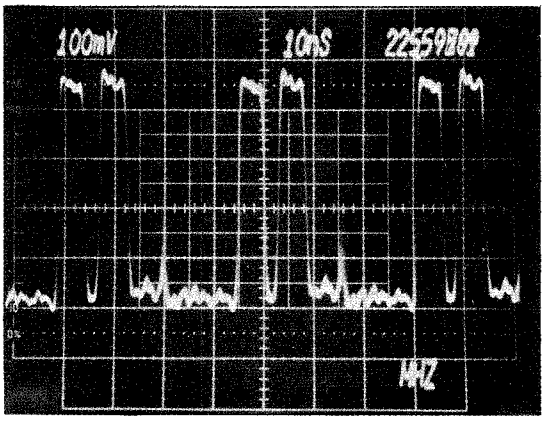

Fig. 4 Multiplexer Data Output (10100000) at 225 MHz Clock Frequency

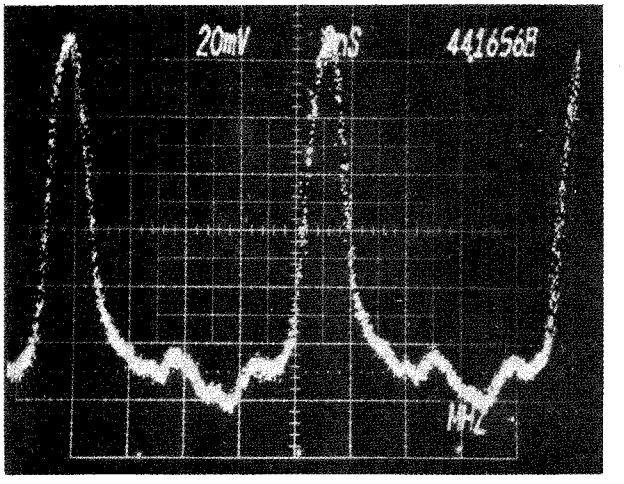

Fig. 6 Demultiplexer Output at 883 MHz Clock Frequency